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10/808,502	03/25/2004	Takehito Tsukamoto	1186.1033	5712

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,502	TSUKAMOTO ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-34 and 52-54* is/are pending in the application.

4a) Of the above claim(s) *4-20,22,23 and 25-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,21,24 and 52-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 9/26/06 has been entered. Applicants have amended claims 1, 21, and 24. Claims 3 and 35-51 are cancelled. Claims 52-54 are newly added.

Claims 1, 21, 24, and 52-54 are treated on the merits in this Office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. (US 5436062).

Regarding claim 1, as shown in figures 6(a-b) and 11-16, Schmidt et al. disclose a multi-layer circuit wiring board (no number) comprising:

(a) a laminate of films 81/19(8)/81 and an adhesive layer 83 (coated metal foil and adhesive, col.15:12-52) for bonding the films,

(b) each film having a wiring pattern 18 (current path, col.10:52-63) formed on at least one surface thereof, wherein the wiring pattern formed on each film is electrically connected with the wiring pattern formed on another film which is disposed neighboring thereto through a via-contact layer 17 (facial connection, col.10:52-63) formed in any one of the neighboring films.

But, Schmidt et al. fail to clearly disclose the films having a thickness of 12.5 μm to 80 μm, and the adhesive layer having a thickness of 30 μm or less.

However, Schmidt et al. disclose that impedance is an important part in an electronic circuit for use in high frequency signals and that the dielectric thickness constancy played an important part. Thus, the thickness (and also the dielectric constant) of the dielectric layer (the film and the adhesive) plays an important role for providing predetermined impedances that are very important for particular applications, especially in high frequency operations.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the films having a thickness of 12.5 μm to 80 μm, and the adhesive layer having a thickness of 30 μm or less in order to achieve a predetermined impedance for a specific application. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Examiner remarks: It is noted that the reference number 18 is designated for all wiring patterned, and 17 is designated for all conductive vias (see figure 16 as one of the final product).

Regarding claim 2, as shown in figure 16, Schmidt et al. disclose the films having almost the same thickness (col.11:43-54).

5. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. in view of Sato et al. (US 5738931).

Regarding claim 52, Schmidt et al. disclose every limitation as shown in claim 1 above, but fail to disclose the wiring pattern that has a tapered surface.

Sato et al., as shown in figures 3A and 4B-4E, disclose a tapered side surface wiring pattern 3 (col.4:1-14) formed on a dielectric layer. Sato et al. further disclose that the shapes of the conductor wiring is depending upon a selected manufacturing process. Therefore, it is merely a matter of choice to have the wiring pattern having tapered surface.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the wiring pattern of Schmidt et al. having tapered surface shape, as taught by Sato et al., in order to reduce cost, because forming a perfect conductive trace line (for example: rectangular shape, which is known to have less skin effect losses) is very difficult to achieve while the tapered surface shape of Sato et al. allows tolerances in etching processes (over etched and under etched for example).

6. Claims 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. (US 5436062) in view of Celaya et al. (US 20020134582).

Regarding claim 21, as shown in figures 6(a-b) and 11-16, Schmidt et al. disclose a multi-layer circuit wiring board (no number) comprising:

(a) a laminate of resin films 81/19(8)/81 and an adhesive layer 83 (coated metal foil and adhesive, col.15:12-52; epoxy resin, col.11:25-28) for bonding the films,

(b) each resin film having a wiring pattern 18 (current path, col.10:52-63) formed on at least one surface thereof, wherein the wiring pattern formed on one resin film (figure 16, center dielectric layer 8) is electrically connected with a wiring pattern 18 (same reference number) formed on another resin film (top/bottom dielectric layer 81) which is disposed next to the one resin film, through a via-contact layer 17 (facial connection, col.10:52-63) provided on the one resin film,

(c) a wiring pattern 18 (top wiring pattern) formed on an outermost resin film (figure 16, top dielectric layer) on one side of the laminate (figure 16, top surface), and

(d) a wiring pattern 18 (bottom wiring pattern) formed on another outermost resin film (bottom dielectric layer) on another side of the laminate (bottom surface).

But, Schmidt et al. fail to disclose the films having a thickness of 12.5 μm to 80 μm and the adhesive layer having a thickness of 30 μm or less, the top wiring pattern is a wiring pattern for mounting an IC, and the bottom wiring pattern is a wiring pattern to be electrically connected with a printed circuit board.

Regarding the films having a thickness of 12.5 μm to 80 μm and the adhesive layer having a thickness of 30 μm or less, Schmidt et al. disclose that impedance is an important part in an electronic circuit for use in high frequency signals and that the dielectric thickness constancy played an important part. Thus, the thickness (and also the dielectric constant) of the dielectric layer (the film and the adhesive) plays an important role for providing predetermined impedances that are very important for particular applications, especially in high frequency operations.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the films having a thickness of 12.5 μm to 80 μm, and the adhesive layer having a thickness of 30 μm or less in order to achieve a predetermined impedance for a specific application. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding the top wiring pattern is a wiring pattern for mounting an IC, and the bottom wiring pattern is a wiring pattern to be electrically connected with a printed circuit board, Celaya et al., as shown in figure 1, disclose an IC package comprising an interposer 12 (a substrate - a circuit board), a circuit pattern 71 (circuit interconnect traces) formed on top surface of the interposer for connecting to IC 20 (semiconductor die), and a circuit pattern 72 (circuit interconnect traces) formed on the bottom surface of the interposer for connecting the interposer to a PCB 30 (a standard PCB), see paragraphs 13-16.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Celaya et al. to have the top wiring pattern formed on an outermost resin film on one side of the laminate of Schmidt et al. is a wiring pattern for mounting an IC (such as IC 20), and the bottom wiring pattern formed on another outermost resin film on another side of the laminate is a wiring pattern to be electrically connected with a printed wiring board (such as the standard PCB 30) in order to place the board of Schmidt et al. in uses and hence providing a complete package.

Regarding claim 24, Schmidt et al. in view of Celaya et al. disclose every limitation as shown in claim 21 above including a multi-layer circuit wiring board (figure 16) mounting an IC (such as IC 20, taught by Celaya et al.), and a printed circuit board (such as the standard PCB 30, taught by Celaya et al.), wherein the multi-layer circuit wiring board comprising:

(a) A first film 8 (center dielectric layer) having a first wiring pattern 18 formed on one surface thereof, a second wiring pattern 18 (same reference number) formed on another surface thereof, and a first via-contact layer 17 electrically connecting the first wiring pattern with the second wiring pattern;

(b) a second film 81 (top dielectric layer) provided with a third wiring pattern 18 (same reference number - top wiring layer) for mounting an IC (such as IC 20, taught by Celaya et al.) on one surface thereof, another surface thereof being superimposed on the one surface of the first film;

(c) a third film 81 (bottom dielectric layer) provided on one surface thereof with a fourth wiring pattern 18 (bottom wiring layer) to be electrically connected with a printed circuit board (such as the standard PCB 30, taught by Celaya et al.), another surface thereof being superimposed on the other surface of the first film;

(d) a second via-contact layer 17 (same reference number) for electrically connecting the first wiring pattern with the third wiring pattern; and

(e) a third via-contact layer 17 (same reference number) for electrically connecting the second wiring pattern with the fourth wiring pattern;

(f) a first adhesive layer 83 for bonding the second film to the first film; and

(g) a second adhesive layer 83 for bonding the third film to the first film,

(h) each of the first, second and third films selectively having a thickness of 12.5 μm to 80 μm and the adhesive layer having a thickness of 30 μm or less.

7. Claims 53-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt et al. and Celaya et al. as applied to claims 21 and 24 above, and further in view of Sato et al. (US 6551124).

Regarding claims 53-54, Schmidt et al. in view of Celaya et al. disclose every limitation as shown in claims 21 and 24 above, but fail to disclose the wiring pattern that has a tapered surface.

Sato et al., as shown in figures 3A and 4B-4E, disclose a tapered side surface wiring pattern 3 (col.4:1-14) formed on a dielectric layer. Sato et al. further disclose that the shapes of the conductor wiring is depending upon a selected manufacturing

process. Therefore, it is merely a matter of choice to have the wiring pattern having tapered surface.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the wiring pattern of Schmidt et al. having tapered surface shape, as taught by Sato et al., in order to reduce cost, because forming a perfect conductive trace line (for example: rectangular shape, which is known to have less skin effect losses) is very difficult to achieve while the tapered surface shape of Sato et al. allows tolerances in etching processes (over etched and under etched for example).

Response to Arguments

8. Applicant's arguments with respect to claims 1-1, 21, and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
11/30/06

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